UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/516,626	11/30/2004	Bernardo De Oliveira Kastrup Pereira	NL02 0444 US	6975

24738 7590 09/20/2006

PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
1109 MCKAY DRIVE, M/S-41SJ
SAN JOSE, CA 95131

EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/516,626	DE OLIVEIRA KASTRUP PEREIRA, BERNARDO	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
9/15/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Application on 11/30/2004.

Priority

3. Receipt of papers submitted under 35 U.S.C. 119(a)-(d) is acknowledged; the papers have been placed on record in the file. The certified copy of 02077168.9, filed on June 3, 2002, has been received and placed on record.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Regarding claims 1 and 10, the claims recite the term "substantially". The term "substantially" is a relative term, which renders the claim indefinite. The term "substantially" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The term "substantially" renders the following phrases indefinite: "executing substantially in parallel", "processing elements

are substantially similar", and "distance ... is substantially the same as" as it is unclear to what degree the executing is in parallel, the processing elements are similar, and the distance the same, respectively.

7. All claims rejected by 35 U.S.C. 112, second paragraph, that have not been specifically addressed above are rejected on the basis of dependence.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by DeHon et al., U.S. Patent No. 5,956,518 (Herein referred to as DeHon).

10. Referring to claim 1, DeHon has taught an integrated circuit comprising:

a plurality of processing elements *[basic functional units (BFUs); component 100]* for executing substantially in parallel at least a subset of a plurality of instructions *[Fig. 4; column 5, lines 3-10, 44-48]*;

issuing means *[F BFUs; See Fig. 4]* for configuring the plurality of processing elements by issuing a program-counter-driven instruction flow *[from the PC BFU; See Fig. 4]* to the plurality of processing elements *[column 5, lines 16-23, 44-48]*; and

configurable interconnection *[programmable interconnect; component 101]* means for connecting each processing element from the plurality of processing

elements to at least a subset of other processing elements from the plurality of processing elements *[Fig. 4; column 5, lines 3-10]*;

characterized in that:

the processing elements from the plurality of processing elements are substantially similar to each other, each processing element from the plurality of processing elements being capable of executing each instruction from the plurality of instructions *[column 5, lines 3-10]*; and

the plurality of processing elements are laid out in a regular grid wherein a distance between a processing element and a neighboring processing element from the plurality of processing elements in a first direction is substantially the same as a distance between the processing element and a neighboring processing element from the plurality of processing elements in a second direction that is different from the first direction *[See Fig. 8; column 8, lines 17-21, 31-37]*.

11. Referring to claim 2, DeHon has taught an integrated circuit as claimed in claim 1, wherein the integrated circuit comprises a very long instruction word processor architecture and the subset of the plurality of instructions comprises a very long instruction word *[column 5, lines 44-48]*.

12. Referring to claim 3, DeHon has taught an integrated circuit as claimed in claim 1, characterized in that the configurable interconnection means connect each processing element to each nearest neighboring processing element in the grid *[column 8, lines 23-30]*.

13. Referring to claim 4, DeHon has taught an integrated circuit as claimed in claim 1, characterized in that the configurable interconnection means comprise bypassing means for bypassing a processing element from the plurality of processing elements *[column 8, lines 38-51].*

14. Referring to claim 5, DeHon has taught an integrated circuit as claimed in claim 1, characterized in that a processing element *[BFU]* from the plurality of processing elements comprises a data storage unit *[memory block; Fig. 6, component 110]*, a function unit *[ALU core; Fig. 6, component 120]* and an internal intercommunication network *[See Fig. 6]* coupling the function unit to the data storage unit *[column 5, line 57 – column 6, line 4].*

15. Referring to claim 6, DeHon has taught an integrated circuit as claimed in claim 5, characterized in that the processing element comprises at least a further unit *[MUX; Fig. 6, component 126]*; the function unit, the further unit and the data storage unit being organized as a very long instruction word processor data path *[When the device is configured to be a very long instruction word (VLIW) system, the MUX, the ALU, and the memory block are all part of the a VLIW processor data path (column 5, lines 44-48; Fig. 4)].*

16. Referring to claim 7, DeHon has taught an integrated circuit as claimed in claim 6, characterized in that the issuing means are distributed over the processing elements *[There are multiple F BFUs. Therefore, the issuing means are distributed over the processing elements (BFUs); See Fig. 4; column 5, lines 44-48].*

17. Referring to claim 8, DeHon has taught a data processing device having an input for receiving a digital data stream and having an output for transmitting a humanly perceptible data result resulting from the digital data stream, chararacterized in that the input is coupled to the output via an integrated circuit as claimed in claim 1, the integrated circuit being arranged for extracting the data result from the digital data stream *[See Fig. 22; column 13, lines 49-67]*.

18. Referring to claim 9, given the similarities between claim 1 and claim 9 the arguments as stated for the rejection of claim 1 also apply to claim 9.

19. Referring to claim 10, given the similarities between claim 3 and claim 10 the arguments as stated for the rejection of claim 3 also apply to claim 10.

Conclusion

20. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gonion et al., U.S. Patent No. 6,094,726, teaches a processor that has multiple cores and a reconfigurable interconnect.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
9/15/2006